

SPECIFICATION

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[CONTROL CHIP WITH MUTLIPLE-LAYER DEFER QUEUE]

Cross Reference to Related Applications

This application claims the priority benefit of Taiwan application serial no. 90127631, filed on November 7, 2001.

Background of Invention

[0001] Field of Invention

[0002] The present invention relates to a control chip having a defer queue and a method of operating the control chip. More particularly, the present invention relates to control chip having a multiple-layer defer queue and a method of operating the control chip.

[0003] Description of Related Art

[0004] At present, personal computer has a central processing unit (CPU) that connects with a control chip through a high-speed CPU bus. The control chip is connected to an AGP bus and one or more PCI buses. The PCI buses may couple with a number of PCI compatible peripheral devices or memory units. Since the CPU is at the core of a personal computer, any requests from the CPU through the PCI bus must be processed quickly and do not affect other requests demanded by the CPU are unaffected. In fact, fast response to a request is one of the factors that indicates the operating efficiency of a computer system.

[0005] Requests sent from the CPU to a PCI bus through the control chip can be grouped together under two major types. The first type includes requests such as input/output

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- [0010] 2. When the CPU issues a request belonging to the first type while the defer bit is still not enabled, due to that the DFQ of the control chip cannot store the first type request, the control chip will repeatedly issue retry response to the CPU. As a result, the CPU repeatedly issues the request to the control chip. This manner reduces the performance and efficiency of the whole system.

Summary of Invention

- [0011] Accordingly, one object of the present invention is to provide a control chip having a multiple-layer defer queue and a method of operating the control chip so that a plurality of first type requests issued from a central processing unit (CPU) can be processed concurrently. Furthermore, the multiple-layer defer queue can support retry and defer transaction at the same time so that the amount of data flow between the CPU and the control chip is greatly reduced and overall performance of the system is improved.
- [0012] The invention also provides a control chip with multi-layer defer queue, coupled to a CPU bus and a PCI bus. The control chip comprises a PCI request queue, which receives a CPU request from the CPU bus, and generating a PCI request record. A multi-layer defer queue respectively responds to the CPU bus by one of a defer response and a retry response when the CPU request is received. A PCI access queue is used to receive the PCI request record. Also and, a PCI controller receives the request from the multi-layer defer queue and causes the PCI request record of the PCI access queue to be transmitted to the PCI bus via the PCI controller. Wherein, when the PCI bus generates a response data and if the CPU request in the multi-layer defer queue is to produce the defer response, then the response data is directly sent to CPU bus. If the CPU request in the multi-layer defer queue is to produce the retry response and the CPU bus issues the CPU request, then the response data is directly transmitted to the CPU bus.
- [0013] In brief, the multiple-layer defer queue facilitates the simultaneous processing of a plurality of CPU requests belonging to the first request type. Furthermore, the multiple-layer defer queue also supports retry and defer transactions. Since the volume of data transmitted between the CPU and control chip is reduced, efficiency and overall performance of the system is greatly improved.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

[0015] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings,

[0016] Fig. 1 is a block diagram showing a control chip having a multiple-layer defer queue therein according to one preferred embodiment of this invention;

[0017] Fig. 2 is a flow chart showing the steps for a control chip having a multiple-layer defer queue therein to process CPU requests picked up from a CPU bus according to one preferred embodiment of this invention; and

[0018] Fig. 3 is a flow chart showing the steps for a control chip having a multiple-layer defer queue therein to process a PCI bus response picked up from a PCI bus according to one preferred embodiment of this invention.

Detailed Description

[0019] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0020] In the following embodiment, a two-layered defer queue is used as an example of the multiple-layer defer queue. However, anyone familiar with the technology knows that the invention is actually applicable to a multiple-layer defer queue having at least two layers.

[0021]

Fig. 1 is a block diagram showing a control chip having a multiple-layer defer queue therein according to one preferred embodiment of this invention. As shown in Fig. 1, the control chip 10 is coupled to a CPU bus 102 and a PCI bus 112. The control

chip 10 at least includes a PCI request queue (PCQ) 106, a multiple-layer defer queue (DFQ) 104, a PCI access queue (PAQ) 108 and a PCI controller (PCIC) 110. The multiple-layer defer queue 104 is able to store a plurality of defer request records, such as two. Each defer request record at least includes an identification code field, an effective data field and a flag field. The PCI request queue 106 and the PCI access queue 108 are able to store a plurality of PCI request records. Each PCI request record at least includes an identification code field. According to the foregoing structure of control chip with multiple-layer defer queue, it can be achieved to have multiple-layer defer queue to simultaneously support transactions of retry and defer by using the identification code field, the effective data field and the flag field.

[0022] When the CPU issues a second-type request at the CPU bus 102, this second-type request is stored in the PCI request queue 106, and the identification code field of the PCI request record will be filled with 00. The code 00 represents that this second-type request does not exit in the multiple-layer defer queue. Then, the control chip responds to the CPU again, causing the CPU to treat the second-type request as one request which has been accomplished. The second-type request together with the PCI request record are shifted to the PCI access queue 108 and wait for the PCI controller 110 to be sent to the PCI bus 112.

[0023] When the CPU issues a first-type request at the CPU bus 102, this first-type request is stored in the PCI request queue 106. If the multi-layer DFQ 104 is fully occupied, the control chip then issues a retry response to the CPU. Then, the identification code field of the PCI request record in the PCI request queue 106 is filled with 00. The code 00 represents that this first-type request does not exit in the multiple-layer defer queue. This first-type request and the PCI request record are not shifted to the PCI access queue 108. In other words, the retry response with respect to the first-type request is not sent by the PCI controller 110 to the PCI bus 112.

[0024] When the multi-layer DFQ 104 inside the control chip is not yet fully occupied, the first-type request is stored the multi-layer DFQ 104 and the PCI request queue 106, and the identification code fields of the DFQ request record and the PCI request record are filled with the same identification code, which is 01 or 10 because the invention has two DFQ layers with different identification codes. Then, according to

whether or not the defer bit in the first-type request is enabled, it is determined to issue a defer response or a retry response to the CPU, which information will be stored in the flag field. After then, the first-type request together with the PCI request record are transferred to the PCI access queue 108 via the PCI request queue 106, and waits for being transmitted to the PCI bus 112 by the controller 110.

[0025] After the first-type request receives the response from the PCI bus and the responded data, wherein the status can be known from the content of 01, 10 in the identification code field, the PCI controller 112 will fill an enable into the effective data field. If the first-type request is a defer response, which can be judged according to the flag field, then the data is directly sent to the CPU and the transaction accomplishes. The first-type request in the multi-layer DFQ 104 is deleted. If the first-type request is a retry response, which can be judged according to the flag field, then the data is temporarily stored in the control chip. When the next identical first-type request is issued by the CPU, then, the data is directly sent to the CPU and the transaction accomplishes. Then, the first-type request in the multi-layer DFQ 104 is deleted.

[0026] Additionally, in order to make the multiple-layer defer queue to simultaneously support transactions of retry and defer, when the CPU issues the first-type request, it is necessary to check whether or not the multiple-layer DFQ 104 has stored the first-type request, which may also be the first-type request of retry response previously issued by the control chip. When it is assured that the first-type request has been stored in the multi-layer DFQ 104, it should proceed another check to see whether or not the data in stored in the multi-layer DFQ 104 at the effective data field has the enable. (I) In the situation of disable, the control chip issues a retry response to the CPU. The identification code field of the PCI request record is filled with 00. This first-type request and the PCI request record are not stored in the PCI access queue 108. (II) In the situation of enable, the control chip will respond to the CPU with the data and the transaction accomplishes. The first-type request stored in the multi-layer DFQ is deleted. The identification code field of the PCI request record is filled with 00. The first-type request and the PCI request record are not shifted to the PCI access queue 108.

[0027] Fig. 2 is a flow chart showing the steps for a control chip having a multiple-layer defer queue therein to process CPU requests picked up from a CPU bus according to one preferred embodiment of this invention. Fig. 3 is a flow chart showing the steps for a control chip having a multiple-layer defer queue therein to process a PCI bus response picked up from a PCI bus according to one preferred embodiment of this invention. The following is a full description of the operation of the control chip with reference to Figs. 1, 2 and 3.

[0028] The control chip 10 receives a CPU request through the CPU bus 102. Then the CPU request is transferred to the PCI request queue 106 for storage (in step s200). If the CPU request is a first-type request, that is, an input/output read request, an input/output write request or a memory read request (in the step s202), then it is checked whether or not the first-type request is existing in the multi-layer DFQ 104 (as shown in step s208).

[0029] When the multi-layer DFQ 104 has stored the first-type request, the effective data field of the request record in the DFQ is checked whether or not is an enable (in step s210). In the situation of disable, the control chip issues a retry response to the CPU (in step s216). The identification code field of the PCI request record is filled with 00 (in step s218) and the request is accomplished. In the situation of enable, the control chip will respond to the CPU with the data and the transaction accomplishes. The first-type request stored in the multi-layer DFQ is deleted (in step s212). The identification code field of the PCI request record is filled with 00 (in step s214) and the request is accomplished.

[0030] When the multi-layer DFQ 104 has not stored the first-type request, and the multi-layer DFQ 104 still has no sufficient storage space (as shown in step s220), then the control chip issues a retry response to CPU (as shown in step s216). Then, the identification code field of the PCI request record is filled with 00 (as shown in step s218), and the request is accomplished.

[0031] When the multi-layer DFQ 104 has not stored the first-type request, and when the multi-layer DFQ 104 still has storage space (in step s220), then an identification code of 01 or 10 is assigned to both of the identification code field of the request record of DFQ and the request record of PCI queue (in step s222). It is judged whether or not

the first-type request can provide defer response (in step s224). If the first-type request can provide defer response, then a defer flag is assigned to the flag field of the request record in DFQ (in step s226). The defer response is responded to CPU bus 102 (in step s228). If the first-type request cannot provide defer response, then a retry flag is assigned to the flag field of the request record in DFQ (in step s230) and the retry response is responded to the CPU bus 102 (in step s232). Then, the PCI request record in the PCI request queue 106 is stored in the PCI access queue 108 (in step s206). After that, the PCI controller 110 takes out the first-type request of the PCI access queue 108 and sends it to the PCI bus 112 (in step 234).

[0032] When the CPU request is a second-type request, that is, a write-in request for the memory, then an identification code of 00 is assigned to the identification code field of the PCI request record in the PCI access queue (in step s204), and an accomplishing response is responded to the CPU bus 102 (in step s236), and the transaction is accomplished. Then, the PCI request record in the PCI request queue 106 is stored into the PCI access queue 108 (in step s206). Afterward, the PCI controller 110 takes out the second-type request of the PCI access queue 108 and sends it to the PCI bus 112 (in step 234).

[0033] When the PCI controller 110 receives a response from the PCI bus 112 and the requested data (in step s310), the PCI controller 110 first judges whether or not the identification code field is filled with 01 or 10 (in step s320). If the identification code is not the 01 or 10, it indicates that the request is a second-type request. If the identification code is 01 or 10, then a DFQ request record with a value in the identification code field being the same as the value of the identification code is searched from the request records in the multi-layer DFQ 104, according to the value of the identification code. Then, the effective data field of the DFQ request record, which has the value in the identification code field being the same as the value of the identification code, is enabled (in step s330). Afterward, the flag field is judged whether it indicates a defer response or a retry response (in step s335). If the flag field of the DFQ request record, which has the value in the identification code field being the same as the value of the identification code, is a defer flag, then the control chip 10 actively sends the requested data to the CPU bus 102. Also and the request record, having the value in the identification code field being the same as the value of

the identification code, is deleted (in step s340). If the flag field of the DFQ request record, which has the value in the identification code field being the same as the value of the identification code, is a retry flag, then the control chip 10 temporarily stores this data until the same first-type request is again issued to the control chip.

[0034] In conclusion, major advantages of this invention includes:

[0035] 1. The system is capable of processing a plurality of first-type requests from the CPU. Moreover, the multiple-layer defer queue supports retry and defer transactions concurrently.

[0036] 2. The amount of data shuttling between the CPU and the control chip is greatly reduced so that the system efficiency and performance is improved.

[0037] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.